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U.S. Serial No. 09/809,772

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J. Artis

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re U.S. Patent Application of:
T. Morayama et al.

Serial No.: 09/809,772 — Examiner: I. Patel

Filed: March 16, 2001 — Group Art Unit: 2841

For: ELECTRONIC CIRCUIT DEVICE

RESPONSE A

Assistant Commissioner for Patents

Washington, DC 20231

Dear Sir:

The remarks below are provided in response to the Office Action dated December 6, 2001. The Commissioner is hereby authorized to charge any deficiency in fees associated with this communication, or credit any overpayment to Deposit Account No. 19-3140.

In The Claims

Please cancel claims 2 and 6.

Please amend claims 1, 3, 4, 5 and 7 as follows:

1. (Once Amended) An electronic circuit device, comprising:

A1 a plurality of circuit boards which have electronic parts mounted thereon, the plurality of circuit boards area stacked in the thickness direction by metal pieces fixed between the circuit boards wherein opposite ends of each metal piece are fixed to opposing circuit boards by materials which have different melting points.

3. (Once Amended) An electronic circuit device, comprising:

a plurality of circuit boards which have electronic parts mounted thereon, the plurality of circuit boards are assembled in the thickness direction by spacers, each spacer comprising a metal piece, and one end of each spacer is fixed to one circuit board by a solder while another

A2 other end of each spacer is fixed to another circuit board by a conductive adhesive agent wherein the conductive adhesive agent has a melting point lower than the solder.

4. (Once Amended) The electronic circuit device as claimed in claim 3, wherein the circuit boards are electrically connected to each other by the spacers.

5. (Once Amended) An electronic circuit device, comprising:

a plurality of circuit boards which have electronic parts mounted thereon, the plurality of circuit boards are assembled in the thickness direction by spacers wherein each spacer comprises a metal piece, and one end of the spacer is fixed to one circuit board by a first solder while another end of the spacer is fixed to another circuit board by a second solder wherein the first solder has a higher melting point than the second solder.

7. (Once Amended) The electronic circuit device of claim 5, wherein the electronic parts

A3 are soldered to the circuit boards by the first solder.

Please add new claims 8-20 as follows:

8. (New) An electric circuit device, comprising:

a plurality of circuit boards;

at least one spacer positioned between the plurality of circuit boards, each spacer having a first surface and a second surface;

a first connector which connects the first surface to one of the circuit boards of the plurality of circuit boards; and

4A a second connector which connects the second surface to another circuit board of the plurality of circuit boards wherein the second connector has a lower thermal characteristic than the first connector which allows the second connector to loosen and separate from the second surface when heat and force are applied to the plurality of circuit boards.

9. (New) The electric circuit device of claim 8, wherein the first connector is a solder.

10. (New) The electric circuit device of claim 8, wherein the first connector is a conductive adhesive agent.

11. (New) The electric circuit device of claim 8, wherein the second connector is a solder.

12. (New) The electric circuit device of claim 8, wherein the second connector is a conductive adhesive agent.

13. (New) The electric circuit device of claim 8, wherein the thermal characteristic is a melting point.

14. (New) The electric circuit device of claim 8, wherein the at least one spacer is tapered.

15. (New) A method of manufacturing an electrical circuit device, comprising:

connecting at least one spacer to a first circuit board by a solder;

applying a conductive adhesive agent to a second circuit board wherein the conductive adhesive agent has a lower melting point than the solder;

pressuring the at least one spacer into the conductive adhesive.

A4 cancel.

16. (New) The method of manufacturing an electrical circuit device according to claim 15, further comprising applying heat to harden the conductive adhesive agent.

17. (New) The method of manufacturing an electrical circuit device according to claim 15, further comprising heating the device to no more than the melting point of the solder and no more than the softening point of the conductive adhesive.

18. (New) The method of manufacturing an electrical circuit device according to claim 15, further comprising separating the first circuit board and the second circuit board.

19. (New) The method of manufacturing an electrical circuit device according to claim 15, wherein the conductive adhesive agent is applied by a printing process.

20. (New) The method of manufacturing an electrical circuit device according to claim 15, wherein the conductive adhesive agent is applied by a transfer plate.

REMARKS

In response to the Office Action dated December 6, 2001, the applicants hereby make the following response. Originally claims 1 - 7 were filed with claims 1, 3 and 5 being independent. In this response, claims 1, 3, 4, 5 and 7 are being amended, claims 2 and 6 are being cancelled and new claims 8-20 are being added with claims 8 and 15 being independent. Applicants respectfully state that no new matter has been added.

Drawings

Figures 9 and 10 have been labeled "Prior Art" in red as suggested by the Examiner.

Rejection Under 35 U.S.C. § 103(a)

Pending Claims 1 and 5 stand rejected under 35 U.S.C. 103(a) as being purportedly obvious over *Akram etl al.* (U.S. Patent No. 5,994,166) in view of *Tokuno et al.* (U.S. Patent No. 5,883,426). Pending Claims 2-4, 6 and 7 stand rejected under 35 U.S.C. 103(a) as being purportedly obvious over *Akram et al.* (U.S. Patent No. 5,994,166) in view of *Tokuno et al.* (U.S. Patent No. 5,883,426) in further view of *Satoh* (U.S. Patent No. 5,276,289). In this response, claims 1, 3, 4, 5 and 7 have been amended, claims 2 and 6 have been cancelled and new claims 8-20 have been added. Applicants respectfully traverse the rejections and request withdrawal of same.

The present invention relates to an electronic circuit device with a plurality of circuit boards sequenced to each other. Between each circuit board is at least one spacer connected to the lower surface of one circuit board and connected to the upper surface of another circuit board (see specification page 8, lines 8-10 and lines 17-19). Each spacer has two ends with one end connected to one circuit board and the other end connected to the other circuit board. Each end

of the spacer connects to the circuit board by materials wherein the material at the first end has a different melting point than the material at the second end (see specification page 4, lines 16-18). The connecting materials may be solder or a conductive adhesive. Thus, the present invention provides a structure wherein the circuit board can be easily disassembled from each other wherein the components can be efficiently and easily re-worked.

As noted by the Examiner, the *Akram* and *Tokuno* references do not teach connecting materials with two different melting points. The primary *Akram* reference teaches multiple stacked substrates wherein the substrates are stacked by column like connections (see column 3, lines 50-52). The electrical connections are formed by techniques such as wire bonds and TAB tape bonding (see column 3, lines 55-59). Thus, in the *Akram* reference, the substrates are in electrical contact via TAB bonds (see column 6, lines 18-21).

The *Tokuno* secondary reference teaches stack modules of semiconductor chips having a heat sink positioned between each semiconductor to relieve thermal stress. In the *Tokuno* reference, connection bumps separate the chips. Accordingly, the *Akram* and *Tokuno* references are not concerned with the disassembly of components as taught by the present invention.

The secondary *Satoh* reference teaches a multi-step electronic circuit device. The *Satoh* reference *specifically* teaches a method which does not utilize wire-bonding or tape carrier bonding (see column 3, lines 17-19 and lines 27-30) as taught by the *Akram* and *Tokuno* references. In the *Satoh* reference, at least four kinds of solder are required by the assembly method (see column 3, lines 62-64). Each solder corresponds to unique elements that make up the substrate. Further, for the at least four kinds of solders of the *Satoh* reference, a difference in melting point between the solders used in one bonding step and the prior bonding step is required to be at least about 10°C (see column 4, lines 15-21). Accordingly, the *Satoh* reference teaches a hierarchy of substrate bonding in the order of increasing melting points (see column 4, lines 42-

45). Thus, the *Satoh* reference is directed to an assembly process which protects prior assembled parts.

The applicants respectfully disagree with the Examiner that the *Akram* reference in view of the *Tokuno* reference in further view of the *Satoh* reference teaches the present invention. The cited references do not teach materials such as solders and conductive adhesives with two different melting points to facilitate the assembly and *disassembly* of the various circuit boards.

The applicants respectfully submit that the Examiner's reference by reference, limitation by limitation analysis fails to demonstrate how the primary *Akram* reference and secondary references teach or suggest their combination to yield the claimed invention wherein the claimed invention has different connecting materials with different melting points for efficient disassembly of the circuitdevice. In contrast, the prior art is never concerned with these issues, and, accordingly, do not discuss or enable same.

Further, to establish a prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art See *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (CCPA 1974). Further, not only must the Examiner find each element of the claimed invention in the prior art, the Examiner must show upon "rigorous application" the proper motivation or suggestion to combine wherein the showing "must be clear and particular" See *In re Dembiczak*, 175 F.3d 994, 999, 50 U.S.P.Q.2d 1614, 17 (Fed. Cir. 1999).

The problem solved by the invention is to facilitate the disassembly of circuit boards for maintenance procedures. Thus, the invention addresses a different problem and proposes a much different solution from the problems and solutions in the art. See, *In re Dembiczak*, 175 F.3d 994, 999, 50 U.S.P.Q.2d 1614, 1617 (Fed. Cir. 1999)(Evidence of a suggestion, teaching or motivation to combine prior art references may flow, inter alia, from the references themselves, the knowledge of one of ordinary skill in the art, or from the nature of the problem to be solved).

In particular, the primary *Akram* reference utilizes wire bonding or TAB bonding to stack devices and does not teach or suggest connecting materials having different melting points.

To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine the reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must be found in the prior art and not based on the applicants' disclosure.

Regarding the first criteria, the cited references do not provide any suggestion to modify the reference to obtain the claimed invention. Instead, the cited references relate to different problems and proposes different solutions than the present invention. One skilled in the art would not be motivated to seek the *Satoh* reference and to combine the *Satoh* reference with the primary reference. As recited in the detailed description of the *Satoh* reference, the *Satoh* reference specifically avoids the wire bonding or tape bonding of the *Akram* reference. Accordingly, one skilled in the art would not seek to combine the references since the references are not compatible.

Regarding the second criteria, the cited references do not provide a reasonable expectation of success. Other than applicants' disclosure, applicants are unaware of any prior uses of the connecting materials with the different melting points. The present invention teaches different materials with different melting points for use as connecting materials to facilitate disassembly of the circuit boards. Unlike the *Satoh* reference, the present invention does not require a determined number of solders with required temperature gradients.

Finally, the cited references do not teach or suggest all the claim limitations of the present invention. The cited references do not teach connecting materials having different melting points as claimed in the present invention.

In order to meet an obviousness requirement, the requirement has to meet some suggestion that the cited references have similar features or structures. To suggest otherwise pertains to an impermissible hindsight reconstruction. The standard, rather, is whether the reference taken as a whole would have suggested the applicant's invention to one of ordinary skill in the plasma display arts at the time the invention was made.

Therefore, Applicants respectfully submit that since claims 1, 3, and 5 are patentable, all dependent claims therefrom are also patentable.

CONCLUSION

In view of the foregoing, it is submitted that all of the pending claims are patentable. Further, the Examiner's rejections have been addressed herein. It is, therefore, submitted that the application is in condition for allowance. Notice to that effect is respectfully requested.

Respectfully submitted,

By its attorney,

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Date: 3/6, 2002

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I hereby certify that this document and any being referred to as attached or enclosed is being deposited with the United States Postal Service as first class mail in an envelope addressed to Assistant Commissioner for Patents, Washington, D.C. 20231, on

3/6/02 Gwen Goldsmith
Date Gwen Goldsmith